CLAIMS

1. A method of creating a stack of integrated circuits selectively connected to provide increased memory density in an application, the method comprising the steps of:

providing a carrier frame configured to have a plurality of members emergent into a window within the carrier frame;

applying a first portion of a solder-containing compound to the first side of the plurality of members;

placing a first packaged integrated circuit having external leads extending away from the packaged integrated circuit in contact with the plurality of members;

processing the first integrated circuit and the carrier frame with a heat source to create a first set of solder connections between the plurality of members and a plurality of the external, extending away, leads of the first packaged integrated circuit;

applying a second portion of a solder-containing compound to the second side of the plurality of members of the carrier frame;

placing a second packaged integrated circuit having external leads extending away from the second packaged integrated circuit in contact with the plurality of members; and

processing the second integrated circuit and the carrier frame with a heat source to create a second set of solder connections between the plurality of members and a plurality of the external, extending away, leads of the second integrated circuit.

2. A circuit module comprised of:

a first packaged integrated circuit in electrical communication with a second packaged integrated circuit, each of the first and second packaged integrated circuits having a peripheral wall, emergent from first and second sides of said peripheral wall are leads that

each have an outer surface and an inner surface;

a plurality of individual contact members for providing the electrical communication between corresponding leads of the first and second packaged integrated circuits, the contact members being configured to have first and second major sides and being disposed to contact on their first major sides, the inner surface of leads of the first packaged integrated circuit and contact on their second major sides, the outer surface of leads of the second packaged integrated circuit, the contact members each having a proximal end and a distal end, the proximal end disposed to point toward the first packaged integrated circuit.

3. The circuit module of claim 2 in which the first and second packaged integrated circuits each have upper and lower surfaces and the upper surface of the second packaged integrated circuit is in contact with the lower surface of the first packaged integrated circuit.

4. The circuit module of claim 2 in which the first and second packaged integrated circuits are separated by a thermal adhesive.

5. The circuit module of claim 2 in which the contact members are composed of lead frame material.

6. The circuit module of claim 5 in which the contact members are composed of alloy 42.

7. The circuit module of claim 2 in which the contact members exhibit a rectangular cross section.

8. The module of claim 2 in which a conductive runner merges with a first selected contact member in contact with a no connect lead of the second packaged integrated circuit to convey a select signal to a chip enable lead of the first packaged integrated circuit.

9. The module of claim 2 in which the first packaged integrated circuit has a bottom surface presenting a lateral extent spanning from a first periphery to a second periphery of the

first packaged integrated circuit, and in which the contact are each disposed so as to not extend into a space bounded on one side by the lateral extent.

10. A high-density memory module comprising:

a first TSOP having a bottom major surface;

a second TSOP positioned in conjunction with the first TSOP to align corresponding leads of the first and second TSOPs;

a plurality of contact members, each contact member having upper and lower major surfaces and each selected contact member being disposed to contact with its upper major surface, the inner surface of a selected lead of the first TSOP and contact with its lower major surface, the outer surface of a corresponding selected lead of the second TSOP, each contact member being disposed outside of a region above and below the bottom major surface of the first TSOP.

11. The module of claim 10 in which the contact between major surfaces of the contact members and the leads of the TSOPs is realized with solder.

12. The module of claim 10 in which the first and second TSOPs are separated by a thermally conductive medium.

13. The module of claim 12 in which the thermally conductive medium is an adhesive.

14. The module of claim 10 in which the contact members are each elongated to have a proximal end and a distal end, the distal end disposed to point substantially away from the TSOPs.

15. The module of claim 10 in which the contact members are each elongated to have a proximal end and a distal end, the proximal end disposed to point substantially toward the TSOPs.

16. A circuit module comprised of:

a first packaged integrated circuit and a second packaged integrated circuit, each of the first and second packaged integrated circuits having an upper surface, a lower surface having a lateral extent, and a peripheral wall, emergent from first and second sides of said peripheral wall are leads that each have a shoulder and foot and an inner surface and an outer surface;

first and second contact members, each having a first major surface and a second major surface, the first contact member being disposed to provide electrical communication between corresponding first leads emergent from first sides of the first and second packaged integrated circuits, respectively and the second contact member being disposed to provide electrical communication between corresponding second leads emergent from second sides of the first and second packaged integrated circuits respectively by contact between the first major surface of the first contact member and the inner surface of the first lead of the first packaged integrated circuit and contact between the first major surface of the second contact member and the inner surface of the second lead of the first packaged integrated circuit while the second major surface of the first contact member is in contact with the outer surface of the first lead of the second packaged integrated circuit and the second major surface of the second contact member is in contact with the outer surface of the second lead of the second packaged integrated circuit to provided electrical communication between the first and second packaged integrated circuits of the module, the first and second contact members being disposed outside of the lateral extent of the lower surface of the first packaged integrated circuit such that the first and second contact members are not disposed above or below any portion of the lower surface of the first packaged integrated circuit.

17. The module of claim 16 in which the contact between the first and second major surfaces of the contact members and the inner and outer surfaces of the first and second leads is electrical contact effectuated by solder.

18. The module of claim 16 in which the upper surface of the second packaged integrated circuit is in contact with the lower surface of the first packaged integrated circuit.

19. The module of claim 16 in which the upper surface of the second packaged integrated circuit is separated from the lower surface of the first packaged integrated circuit by thermal media.

20. The module of claim 16 in which the first and second contact members are elongated and have proximal ends pointing substantially toward the first or second integrated circuit.

21. The module of claim 20 in which the proximal ends point toward the first integrated circuit.

22. A circuit module comprised of:

a first packaged integrated circuit in electrical communication with a second packaged integrated circuit, each of the first and second packaged integrated circuits having a peripheral wall, emergent from first and second sides of said peripheral wall are leads that each have an outer surface and an inner surface;

a plurality of individual contact members for providing the electrical communication between corresponding leads of the first and second packaged integrated circuits, the contact members being configured to have first and second major sides and being disposed to contact on their first major sides, the inner surfaces of leads of the first packaged integrated circuit and contact on their second major sides, the outer surfaces of leads of the second packaged integrated circuit, the contact members disposed outside of a respective

proximal plane extending along and perpendicular to a respective proximal lateral edge of a lower surface of the first packaged integrated circuit.

23. The circuit module of claim 22 in which the first and second packaged integrated circuits each have upper and lower surfaces and the upper surface of the second packaged integrated circuit is in contact with the lower surface of the first packaged integrated circuit.

24. The circuit module of claim 22 in which the first and second packaged integrated circuits are separated by a thermal adhesive.

25. The circuit module of claim 22 in which the contact members are composed of lead frame material.

26. The circuit module of claim 25 in which the contact members are composed of alloy 42.

27. The circuit module of claim 22 in which the contact members exhibit a rectangular cross section.

28. The module of claim 22 in which a conductive runner merges with a first selected contact member in contact with a no connect lead of the second packaged integrated circuit to convey a select signal to a chip enable lead of the first packaged integrated circuit.